Claims: Please amend the claims according to the status designations, which contains all claims that were ever in the application, with the text of all active claims. In addition, since it is recommended that all claims commence at the start of a new page, the claims section within the application that was appended to the end of page 17 should start at the beginning of page 18.

1. (Currently Amended) A method by which on the output of a dc to ac inverter when used in producing a modified sine wave is clamped to a midpoint level between the voltages used within thereby providing an output waveform that remains consistent and independent of any given load comprising:
   (a) a dc to dc converter that produces high differential voltages from the input of the said dc to ac inverter;
   (b) a half bridge configured converter capable of supporting full power using three terminal semiconductor devices and using the said high differential voltages in (a);
   (c) a pulse width modulator function as used to generate the said high differential voltages outputted from the said dc to dc converter in (a) producing a clock frequency that is a multiple of the output said modified sine wave frequency;
   (d) a clock generator function that divides down the operating frequency of the said pulse width modulator in (c) to the said output said modified sine wave frequency;
   (e) a pulse wave shaper function that accepts a single input from the said clock generator in (d) and provides drives for the said three terminal semiconductor devices used within the said half bridge configured converter;
   (f) a snubber pulse generator function that accepts inputs from the said pulse wave shaper function in (e) and provides drives for two said three terminal semiconductor devices;
   (g) a transformer having three magnetically coupled windings whereby two of the three windings are driven by the said snubber pulse generator in (f); and
   (h) a filtering function that accepts its input from one winding of the said transformer in (g) and has its output connected to the input of the said dc to ac inverter.

2. (Currently Amended) A transformer able to operate at a high switching frequency and at a medium to high power level with two low impedance primary windings magnetically coupled to one low impedance secondary winding wherein each primary winding has current passing within it when its associated three terminal semiconductor device closes the circuit.

3. (Currently Amended) The transformer as claimed in 2 further comprising the characteristics wherein both of the said low impedance primary windings have an identical quantity of turns, are wound in an opposing manner to one another and the said one low impedance secondary winding is wound with the same sense of only one primary winding.

4. (Currently Amended) The transformer as claimed in 2 further comprising the characteristics wherein each low impedance primary winding is magnetically coupled to the common said one low impedance secondary winding and for each positive voltage alternately induced across each said low impedance primary winding will produce a positive voltage across the common said one low impedance secondary winding that is synchronously resistively loaded thereby declaring that the said transformer is operating in the forward converter mode.

5. (Currently Amended) The transformer as claimed in 2 further comprising the characteristics wherein the said one low impedance secondary winding having its output rectified, filtered, and connected to the source input of the said dc to ac inverter thereby creating a non-dissipative load with efficient utilization of transformed energy and simultaneously reflecting back to the said low impedance primary winding a lower impedance for actively snubbing transients incurred by an output inductive load only for the duration of the output said modified sine wave deadtime.

6. (Currently Amended) Two independent directional diodes alternately biased at a high frequency for a duration in time within the said output said modified sine wave deadtime and both connected to the load whereby only one diode of the two permits current flow through its associated said primary winding of the said transformer mentioned in claim 2 pending the polarity of any transient as induced by an inductive load within the same said modified sine wave deadtime.

7. (Currently Amended) A high frequency snubber pulse generator mentioned in claim 1 that provides two outputs of which each output provides 50 or more pulses and less than 500 pulses coincidental with the said output said modified sine wave deadtime.

8. (Currently Amended) The high frequency snubber pulse generator of claim 7 further comprising a self oscillating circuit that outputs a succession of identical said pulses at a duty cycle no greater than fifty percent and for each pulse provide transition times with very high slew rates in order to sustain the pulse wave shape.

9. (Currently Amended) The high frequency snubber pulse generator of claim 7 further comprising the supply voltage and return used for creating self oscillation be obtained from the input source voltage to the said dc to ac inverter yet provide power and ground isolation when driving the output said three terminal semiconductor devices.

10. (Currently Amended) The high frequency snubber pulse generator of claim 7 further comprising an output drive that can support the controlling terminal of the said three terminal semiconductor device without distortion to the output said pulses and result with enough current capability of each said three terminal semiconductor device so that the ramping current determined by its associated said one low impedance primary winding will attain its final value.

11. (Currently Amended) The high frequency snubber pulse generator of claim 7 further comprising the characteristics wherein the succession of said identical said pulses from either of the said two outputs is initiated and coincidental with the turning off of either of the two said three terminal semiconductor devices used within the said half bridge converter.

12. (Currently Amended) The high frequency snubber pulse generator of claim 7 further comprising the characteristics wherein the output gating initiates the said output said pulses from either of the said two outputs at a time no less than one half cycle of the said high frequency snubber pulse generator frequency in order to accommodate turn off times of said either of the two said three terminal semiconductor devices used within the said half bridge converter.

13. (Currently Amended) The high frequency snubber pulse generator of claim 7 further comprising the characteristics wherein the said output gating initiates the sequence of the said output said pulses in the low state with minimal delay when driving any said three terminal semiconductor device.